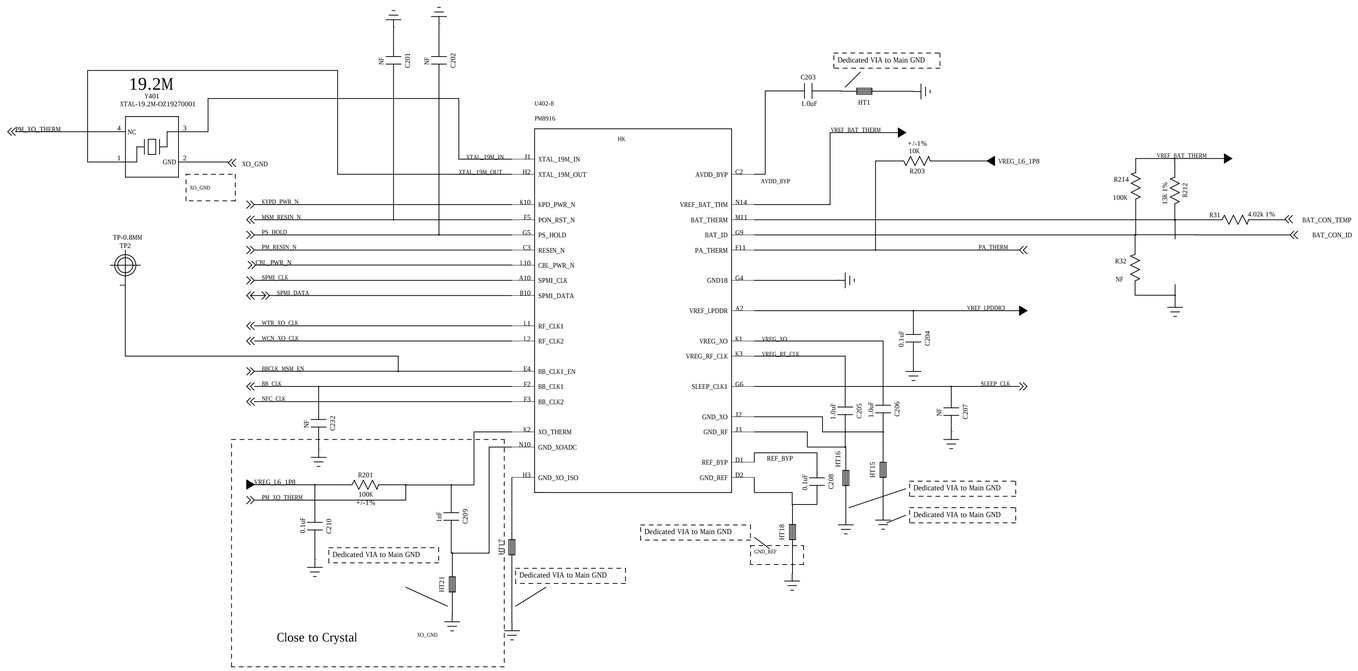

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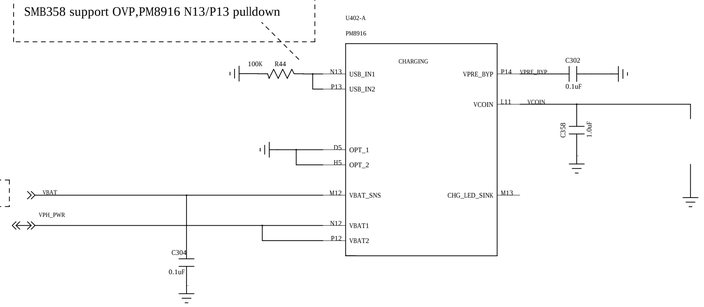
Pins	Hi Z	GND
OPT_1	No SMB1360	SMB1360 present
OPT_2	No Ext APC buck (S5)	Ext APC buck (S5) present

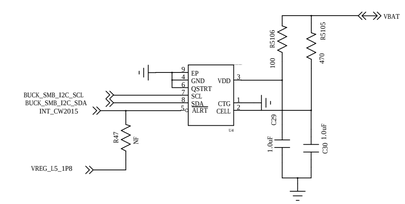
SMB358 support OVP,PM8916 N13/P13 pulldown

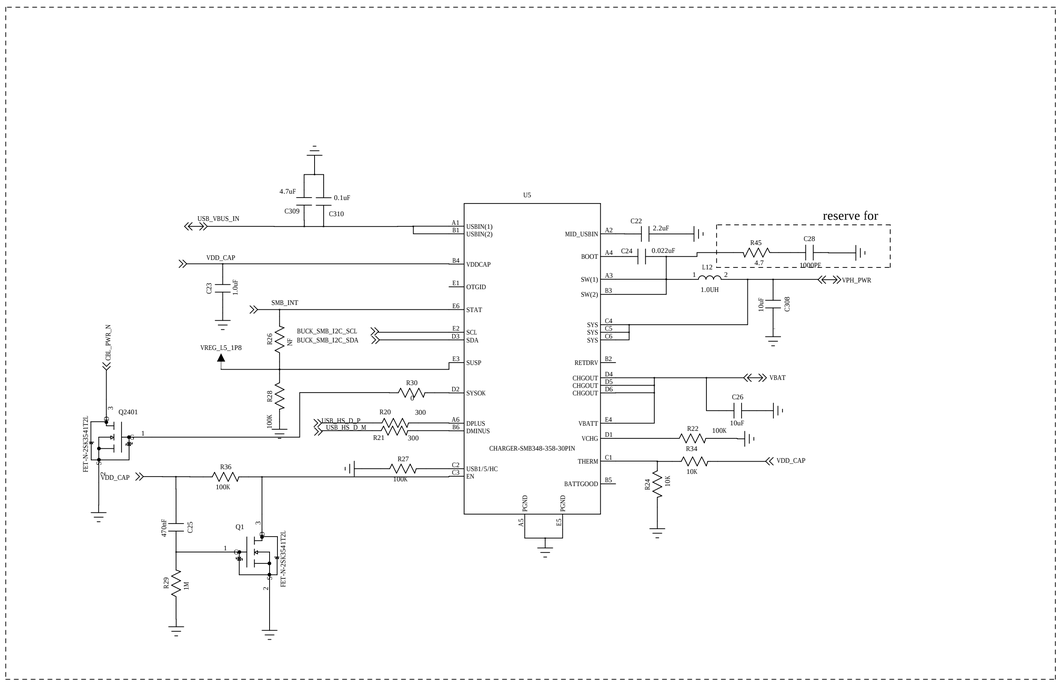


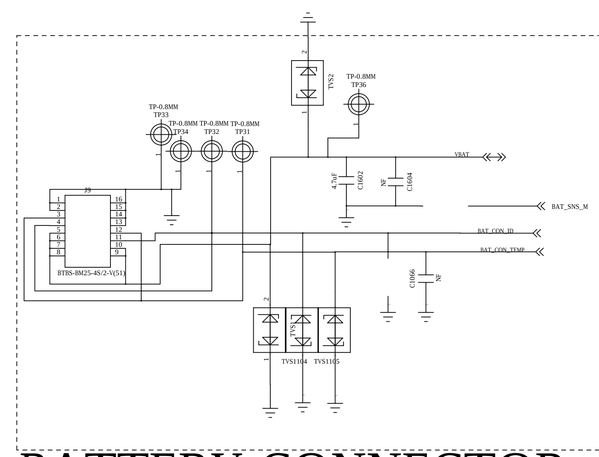
Dedicated sense trace to battery connector

Already have 47K resistor in subboard

Close to connector
if using PMIC's linear charger
C0301 should assemble 4.7uF/16V capacitor
R0307 should assebble 0 ohm
R0302 should NC
R0312 should be 0ohm
BAT THERM switch to PM8916







BATTERY CONNECTOR

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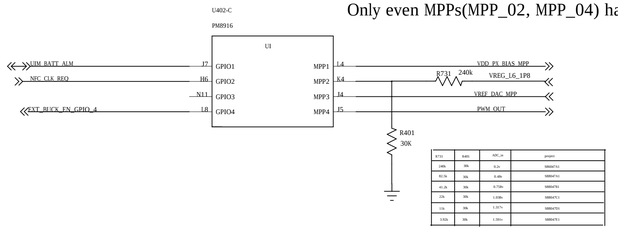
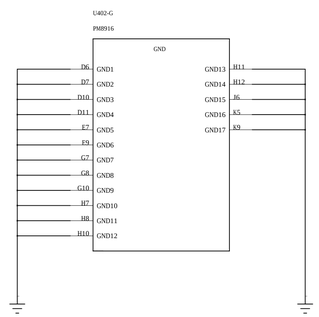
Only odd MPPs (MPP_01, MPP_03) can be configured as analog outputs.
Only even MPPs(MPP_02, MPP_04) have current sink capability.



R731	R401	MPP_01	proper
240k	30k	0.2v	600mV/x1
92.5k	30k	0.4v	600mV/x1
41.2k	30k	0.75v	600mV/x1
15k	30k	1.05v	600mV/x1
1.5k	30k	1.575v	600mV/x1
13.5k	30k	1.35v	600mV/x1



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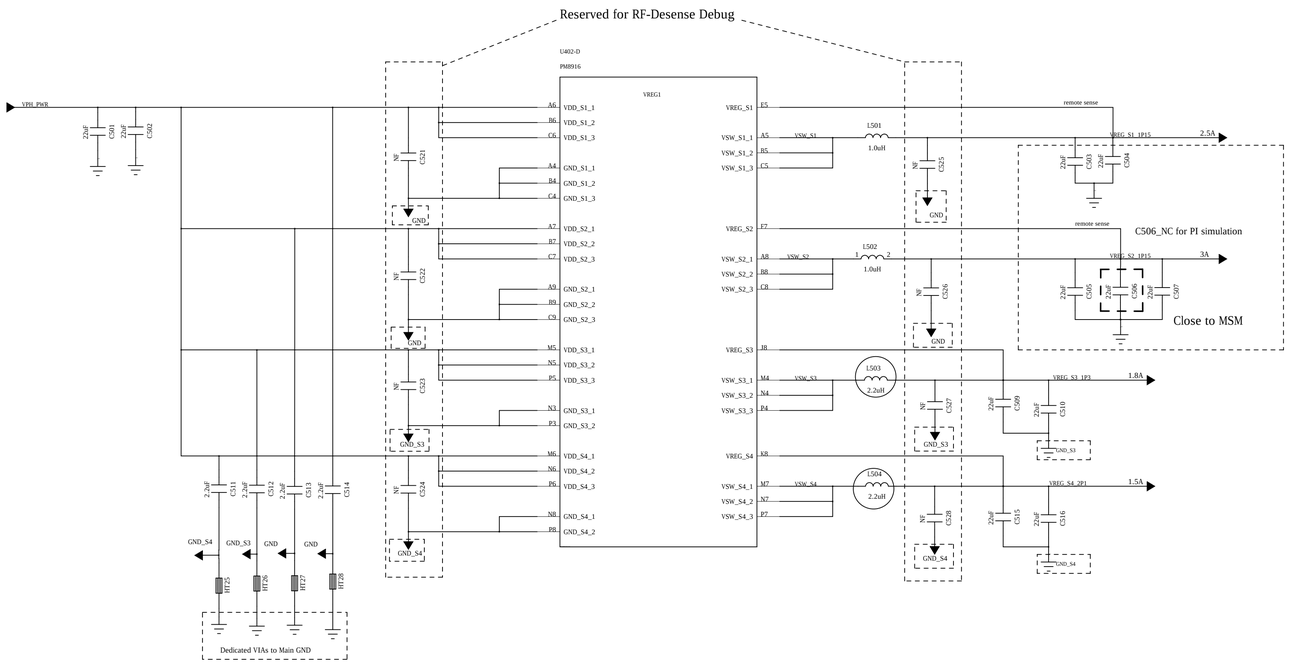

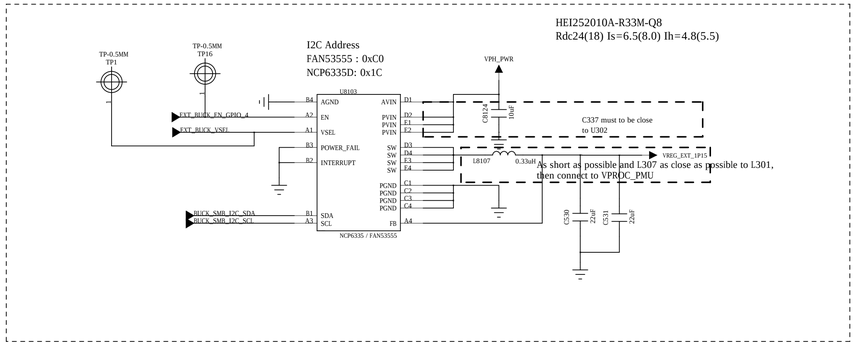

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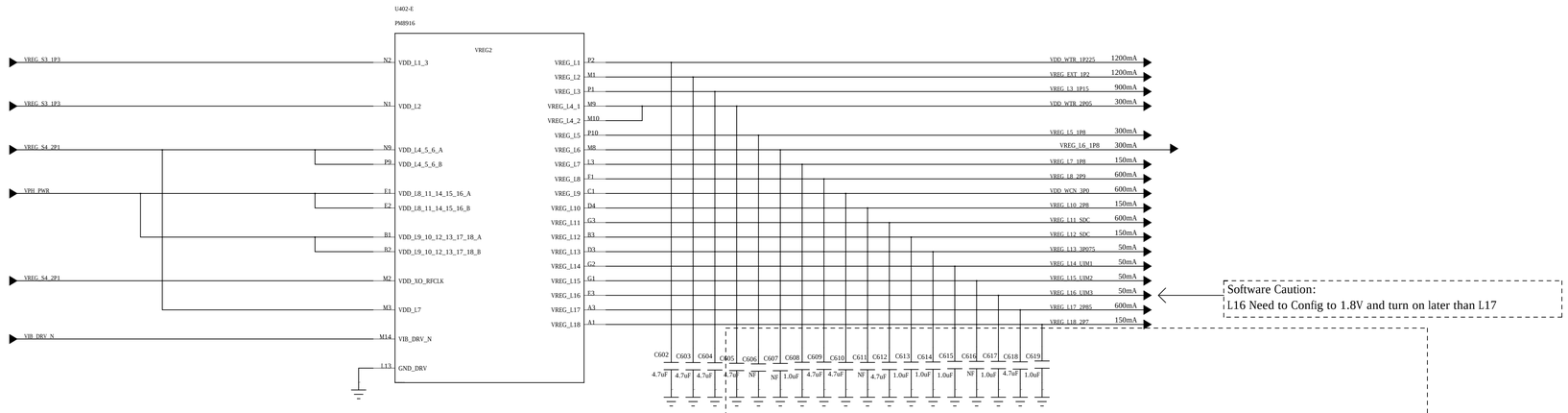

Software Caution:
L16 Need to Config to 1.8V and turn on later than L17

PSEUDO CAPLESS LDOs
L4, L5, L6, L7, L8, L9, L10, L11, L12, L13, L14, L15, L16, L17, L18

Local output capacitor can NC/Remove depends on remote load capacitors and PCB layout
LDOs L8, L9, L11, L17 each shall have total effective output capacitance of 4.7uF.
Please refer to PM8916 training slides(80-NK808-21) for limits on LDO output trace resistance and inductance
Rest of the LDOs shall each have total effective output capacitance of 1.0uF.

The Pseudo capless LDOs must comply to following tolerable routing requirement:
P50: R<400mOhms, L<45nH
P150: R<200mOhms, L<20nH
P300: R<150mOhms, L<18nH
P600: R<150mOhms, L<18nH

Please ensure when you DNI the output capacitor of Pseudo capless LDOs
the effective total capacitance at load side shall match above requirement

NC first

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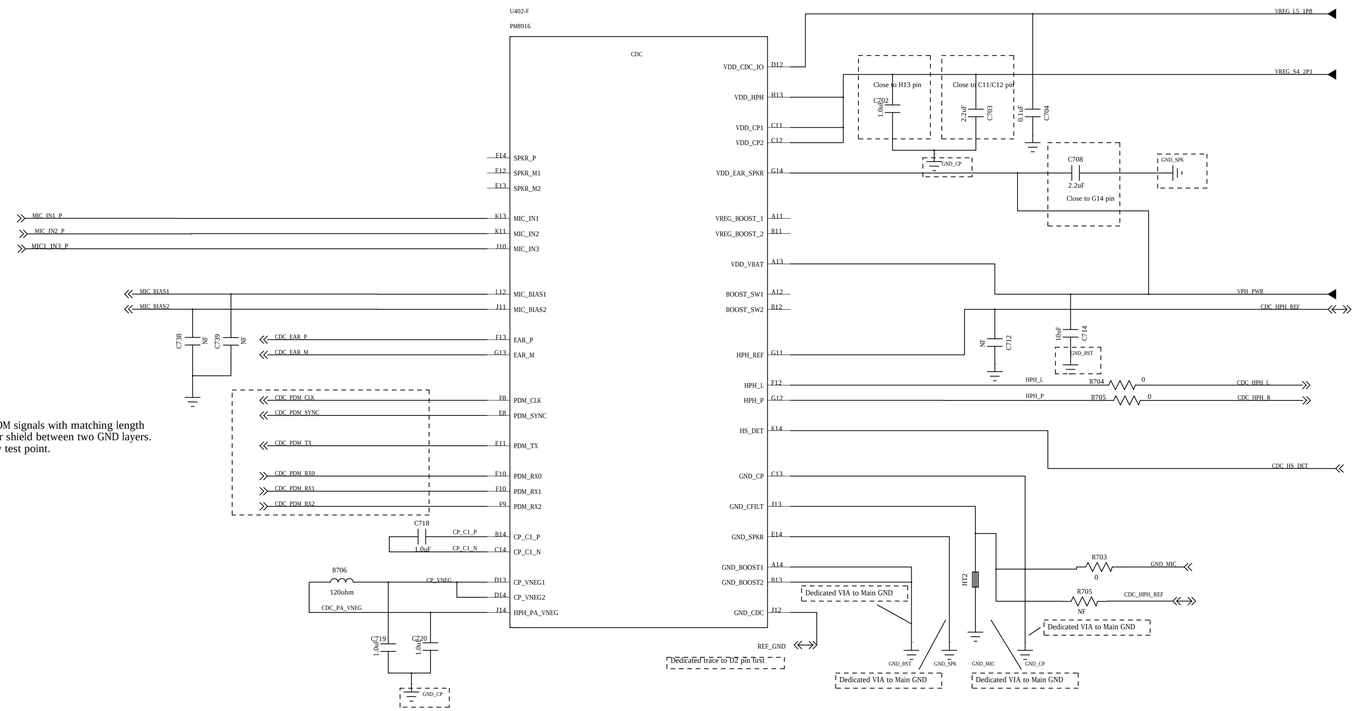

Route codec PDM signals with matching length
on a inner layer shield between two GND layers.
Do not add any test point.

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For BBCLK1,AD35 will be the first load and AL34 will be the final load
Should be a daisy chain route

3620 vs 3680B
R450 NF 0
R451 0 NF

U401-A

CONTROL

CLK_OUT	AR8	WLAN_XO
BB_CLK	AL34	CXO
BBCLK_MSM_EN	A36	CXO_EN
SLEEP_CLK	G36	SLEEP_CLK
MSM_RESIN_N	F35	RESIN_N
MSM_RESOUT_N	AV1	RESOUT_N
	AU32	MODE_0
	AT31	MODE_1
PS_HOLD	F36	PS_HOLD
JTAG_RESOUT_N	K1	SRST_N
JTAG_TCK	M1	TCK
JTAG_TDI	M3	TDI
JTAG_TDO	P2	TDO
JTAG_TMS	L2	TMS
JTAG_TRST_N	K3	TRST_N
VREF_LPDDR3	J12	EBI_VREF_CA
	H21	EBI_VREF_D0_D2
VREF_LPDDR3	J26	EBI_VREF_D1_D3
	AN8	DNC1
	BA36	DNC2
	AY35	DNC3

R450 0 NF
R451 0 NF

TP8 TP-0.8MM
TP26 TP-0.8MM

Star routing from C0803 to PINs
NC others CAPs first

NF C0801 NF C0802 0.1uF C0803

SDC1_CLK	AE36	SDC1_CLK
SDC1_CMD	AH35	SDC1_CMD
SDC1_DATA_0	AD37	SDC1_DATA_0
SDC1_DATA_1	AF38	SDC1_DATA_1
SDC1_DATA_2	AG34	SDC1_DATA_2
SDC1_DATA_3	AH37	SDC1_DATA_3
SDC1_DATA_4	AG40	SDC1_DATA_4
SDC1_DATA_5	AG38	SDC1_DATA_5
SDC1_DATA_6	AF39	SDC1_DATA_6
SDC1_DATA_7	AF35	SDC1_DATA_7
SDC2_CLK	R4	SDC2_SDCARD_CLK
SDC2_CMD	N6	SDC2_SDCARD_CMD
SDC2_DATA_0	P3	SDC2_SDCARD_D0
SDC2_DATA_1	R6	SDC2_SDCARD_D1
SDC2_DATA_2	T7	SDC2_SDCARD_D2
SDC2_DATA_3	P7	SDC2_SDCARD_D3
USB_HS_DM	AC40	USB_HS_D_M
USB_HS_DP	AB39	USB_HS_D_P
NC46	AA40	
USB_HS_REXT	AC38	USB_HS_REXT
USB_HS_SYSCLOCK	AD35	BB_CLK
PMIC_SPMI_CLK	AK37	SPMI_CLK
PMIC_SPMI_DATA	AJ36	SPMI_DATA

R802 0

Close to MSM

R804 0

R803 200 +/-1%

SPMI Data trace length should be within +/-2mm of SMPI Clock trace length. 33pF shunt caps must be no more than 2mm away from the MSM.

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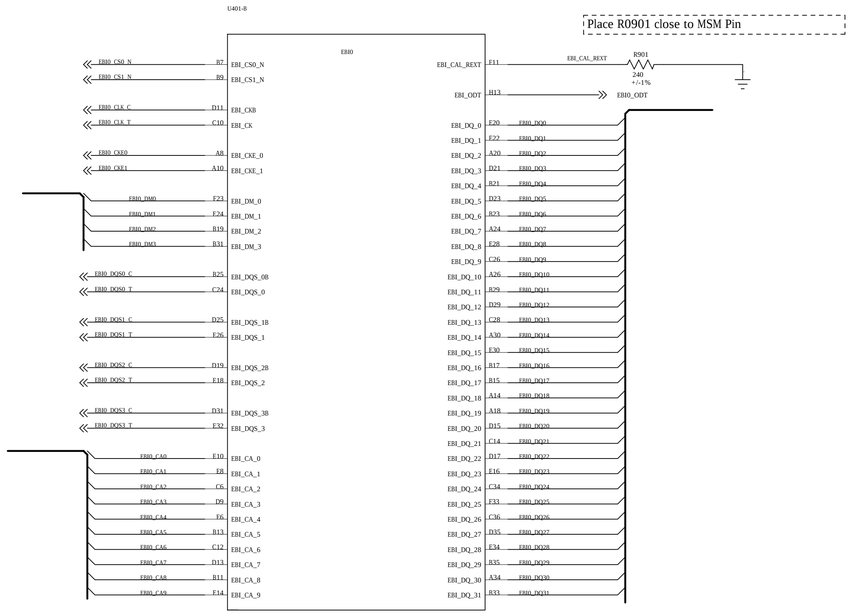

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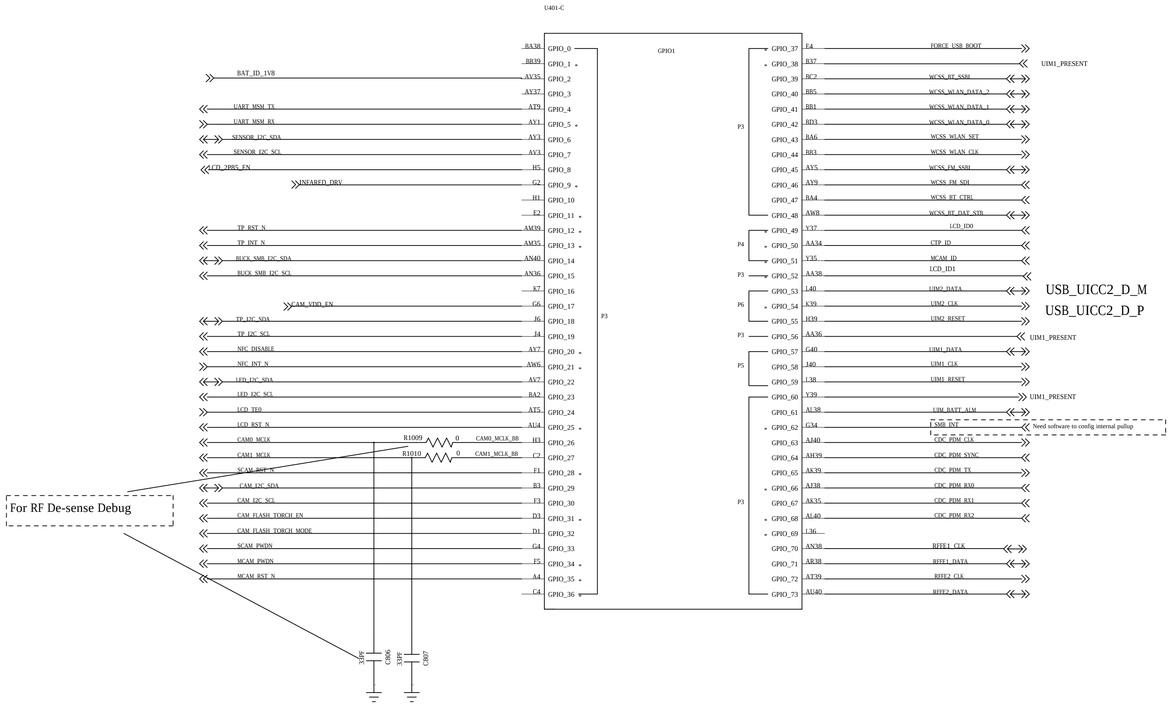

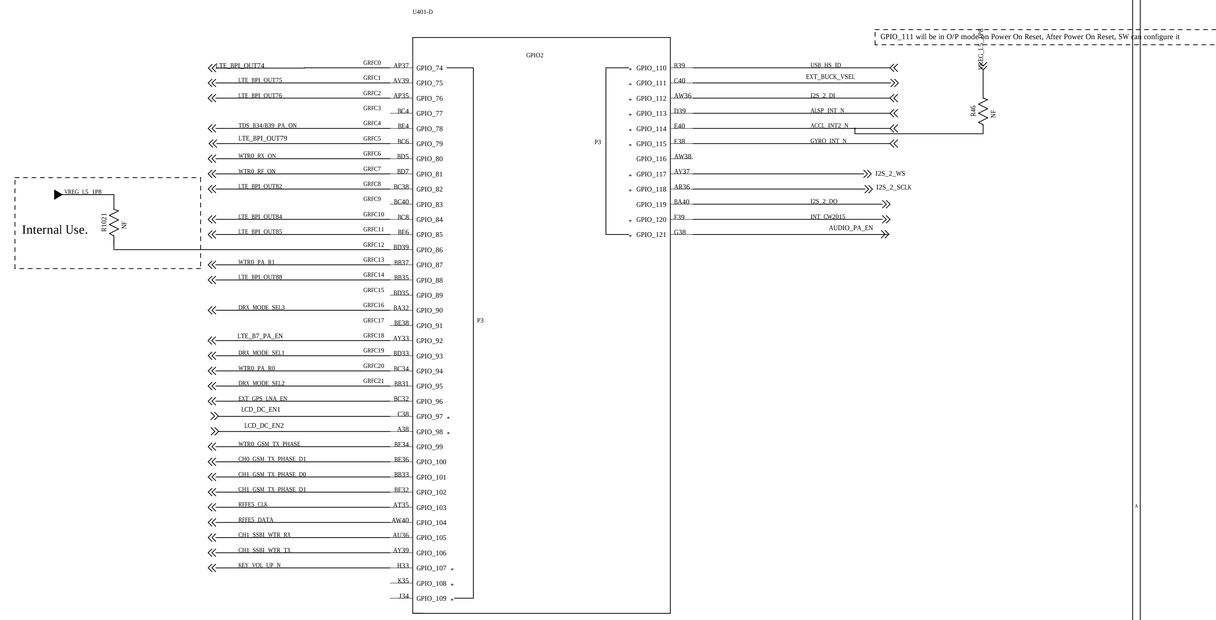

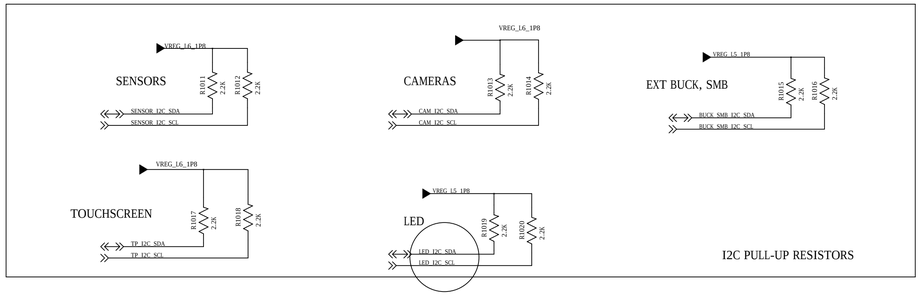

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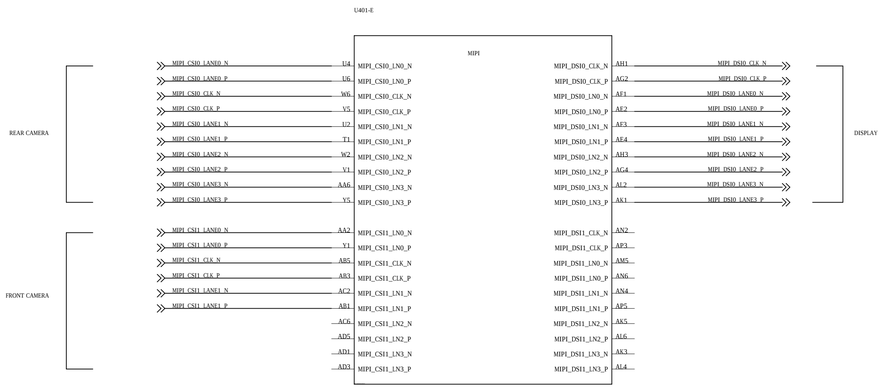

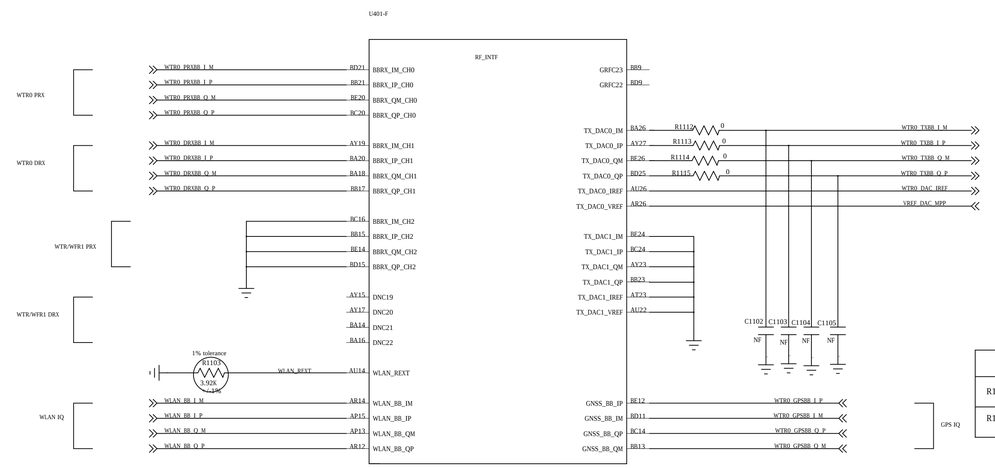

	SVLTE,DSDA	OTHERS
R1102	0OHM	NC
R1120	NC	0OHM

These NC resistor is for SVLTE or DSDA. Change them to 0ohm on other modes.

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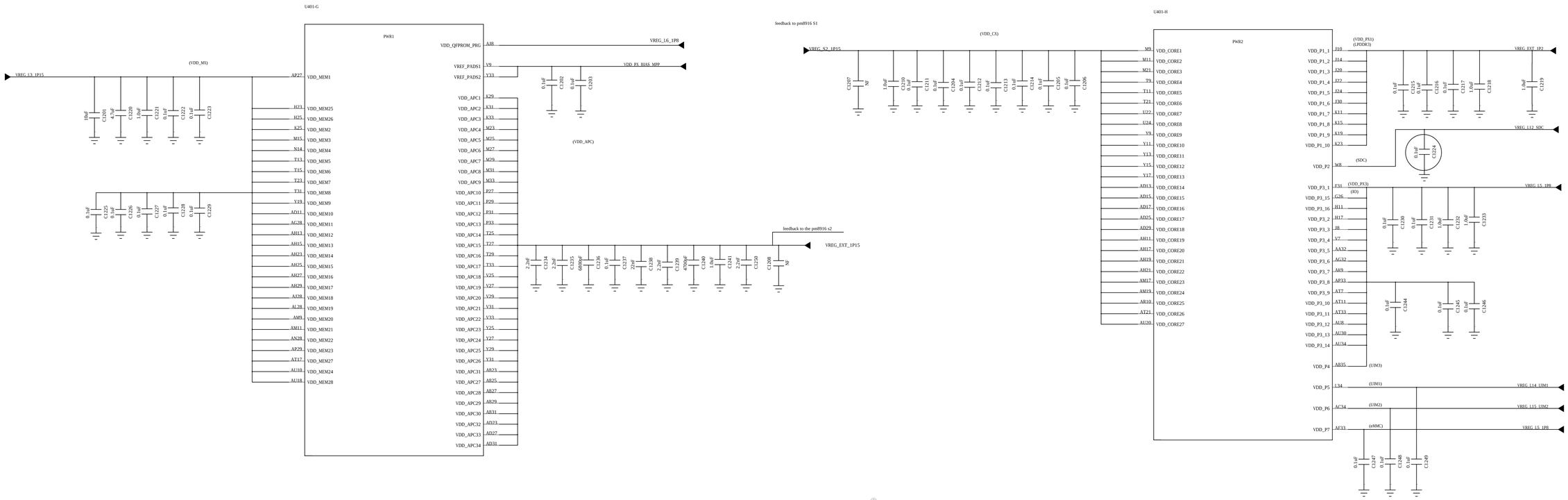

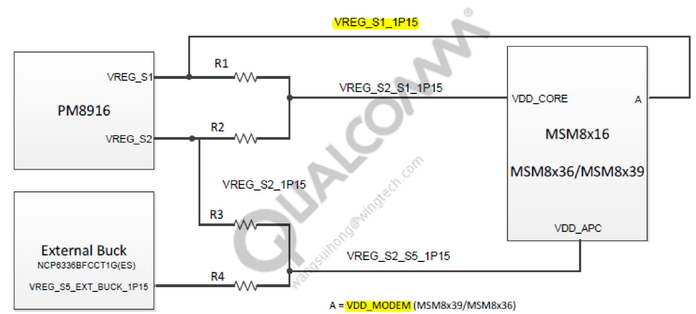

SoC	Jumper on	Jumper off
MSM8x16	R1, R3	R2, R4
MSM8x36/MSM8x39	R2, R4	R1, R3

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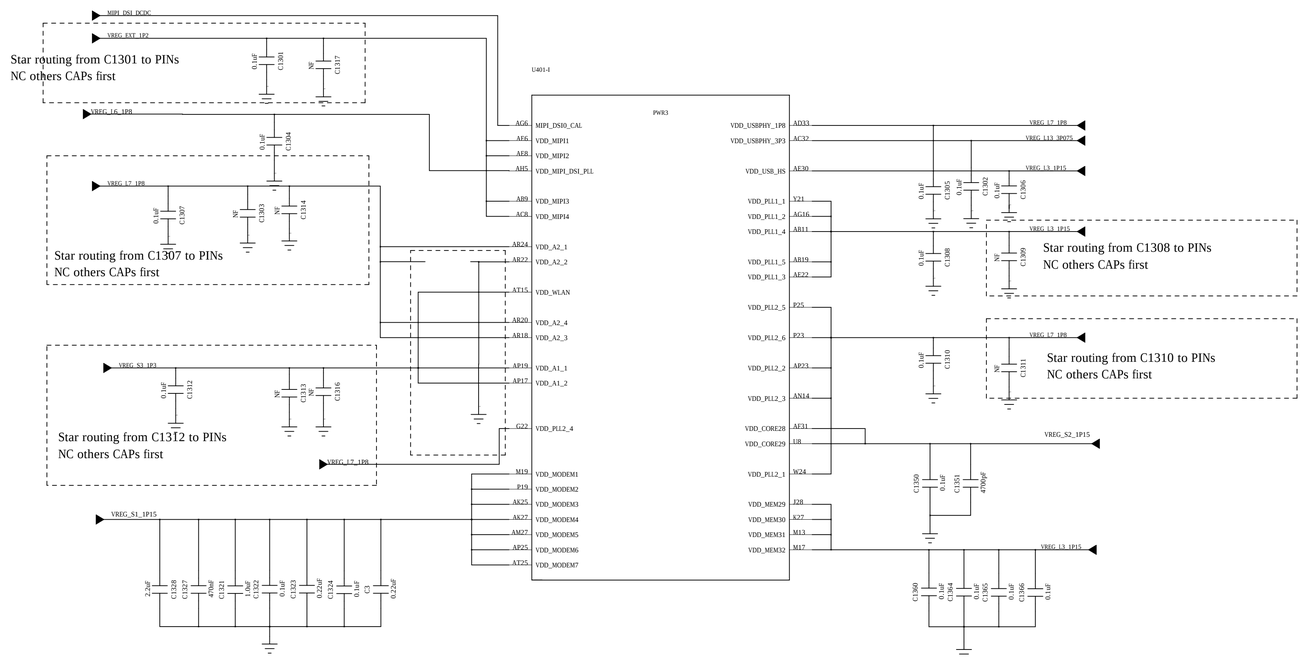

	SVLTE,DSDA	OTHERS
R1301	0OHM	NC
R1302	NC	0OHM

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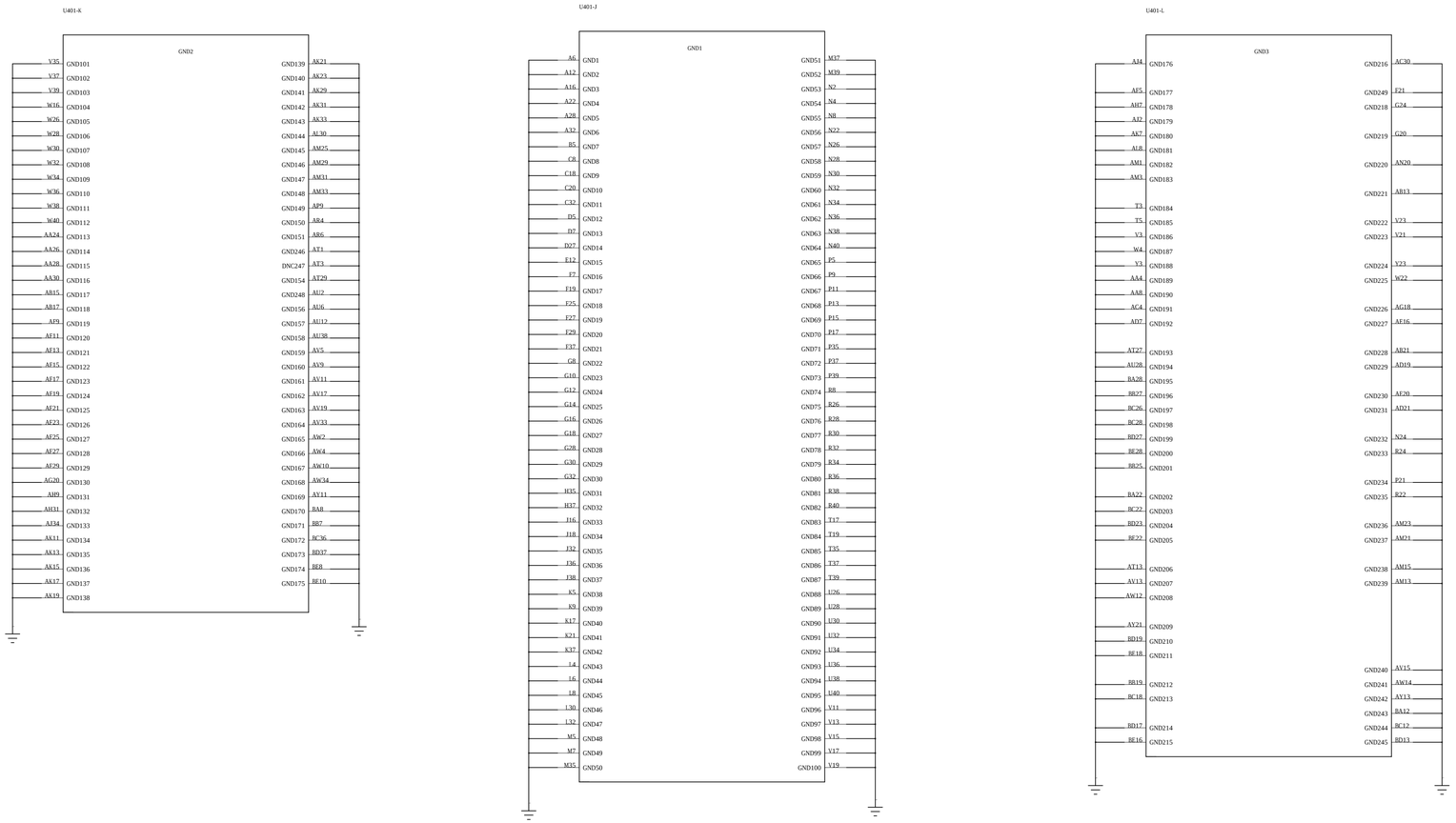

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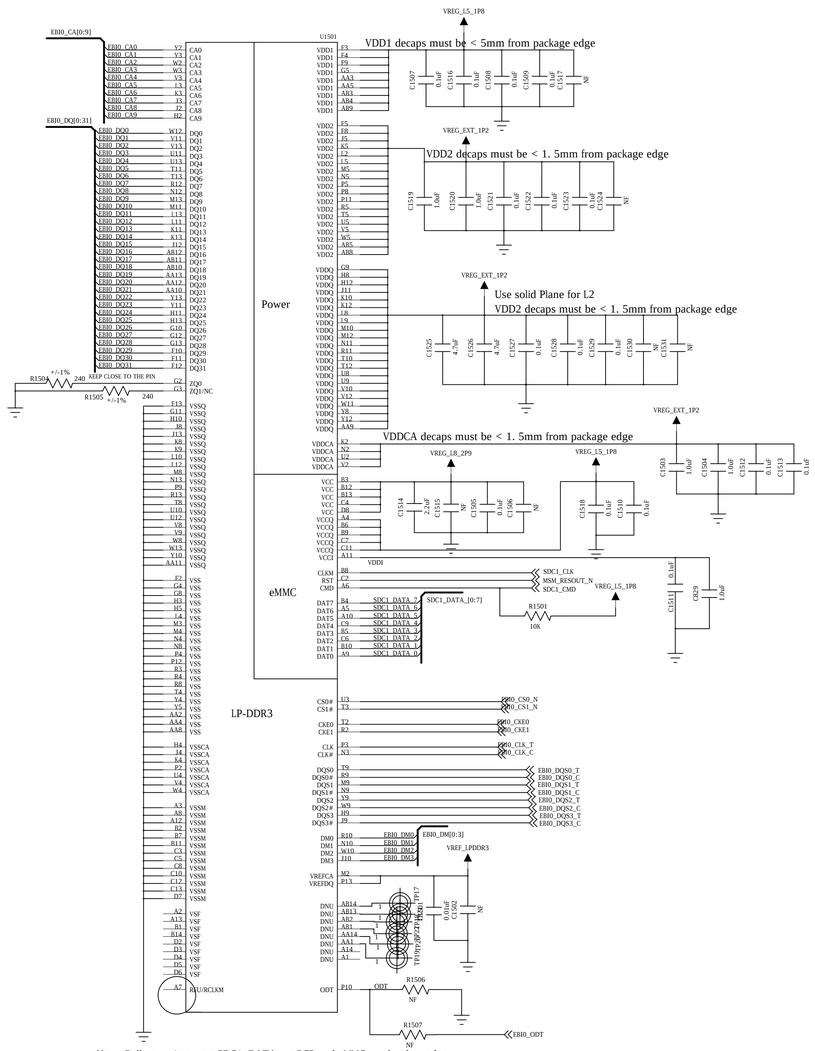

	MICRO/HYNIX	SAMSUNG
U1501.G3	ZQ1	NC
U1501.A7	RFU	RCLK

Note: Pull-up resistors on SDC1_DATA are PCB and eMMC vender dependent

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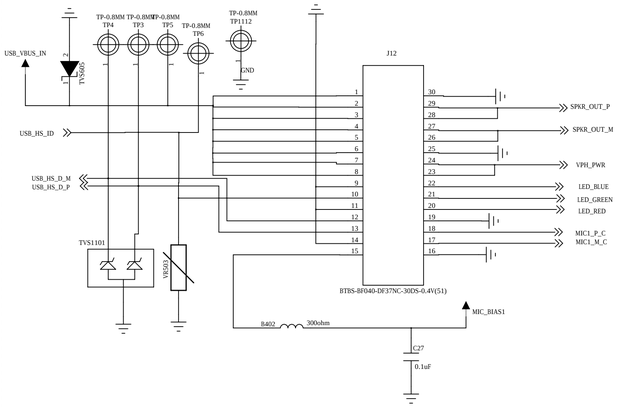
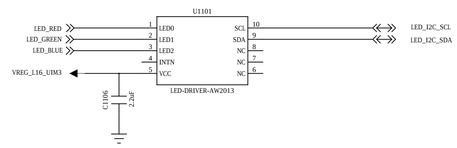


M-MIC+USB+RGB+SPK



RGB

I2C Address	
Write	8B0x8A
Read	8B0x8B

Power on sequence: can be applied in any order

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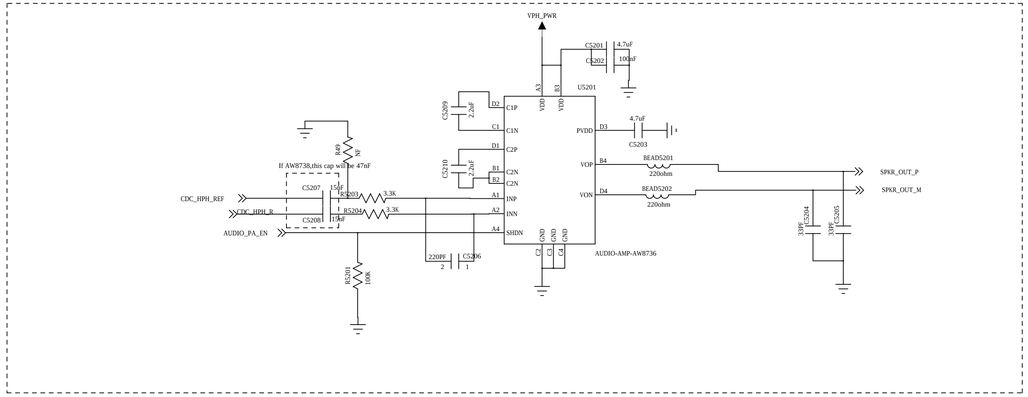

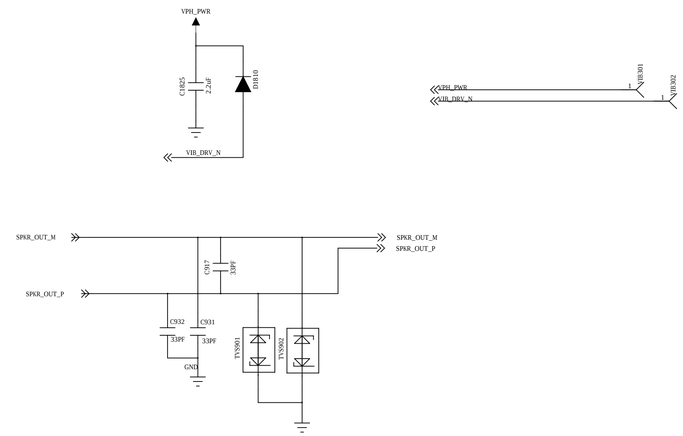

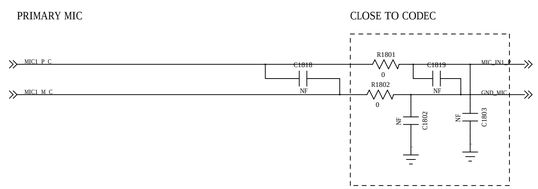

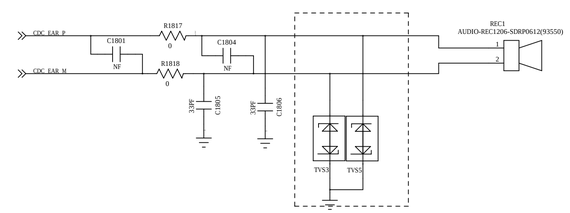

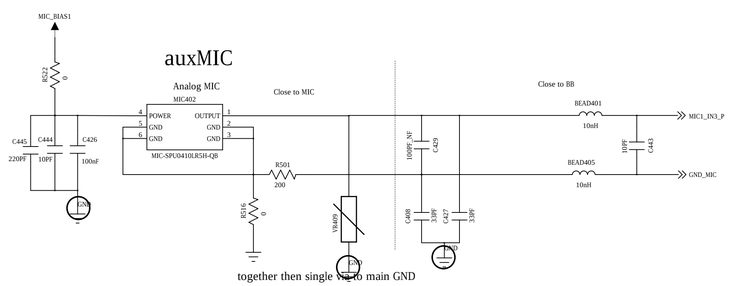

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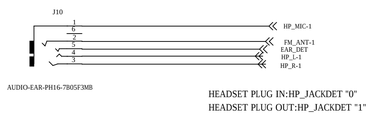
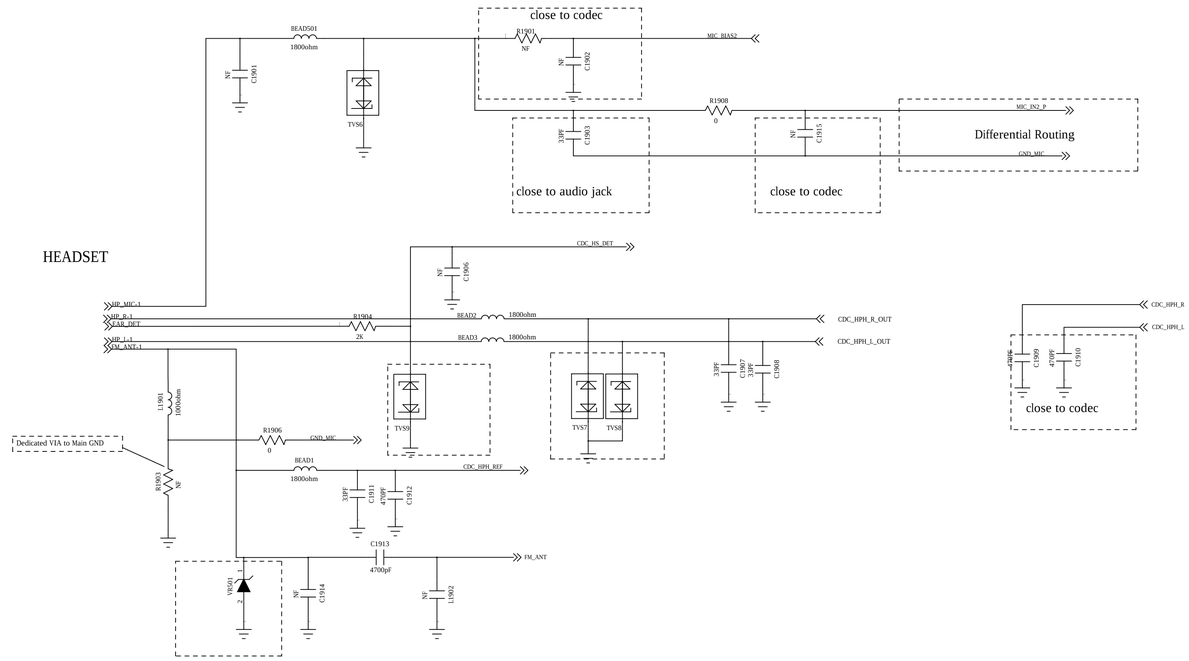
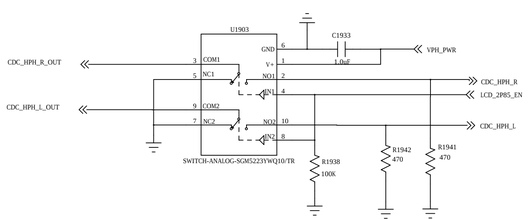


HEADSET PLUG IN:HP_JACKDET "0"
HEADSET PLUG OUT:HP_JACKDET "1"





IN=0, COM Connected to NC;
IN=1, COM Connected to NO;

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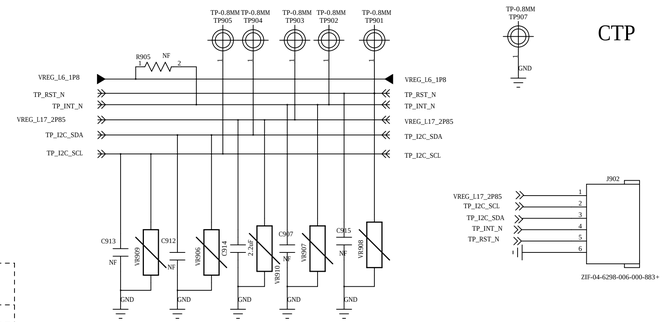
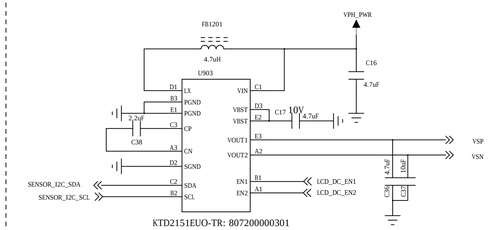


CTP

Power on sequence: Single Supply

FocalTech: FT5336

I2C Address		
Write	0x70	It can be changed by FACTORY.
Read	0x71	

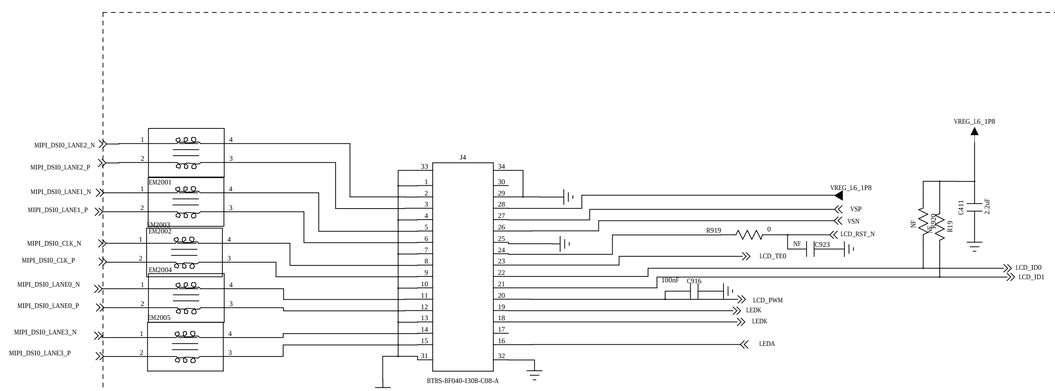


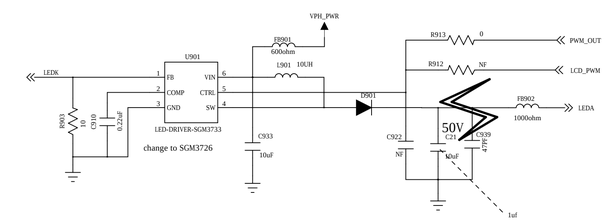
KTD2151 powers ON with a default voltage of 5.4V

SBL software should configure this to 5.0 V

LCD

5.0' FHD





Backlight LED Driver

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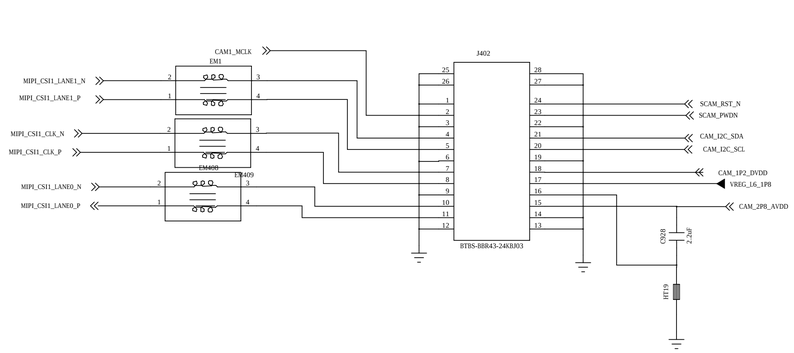
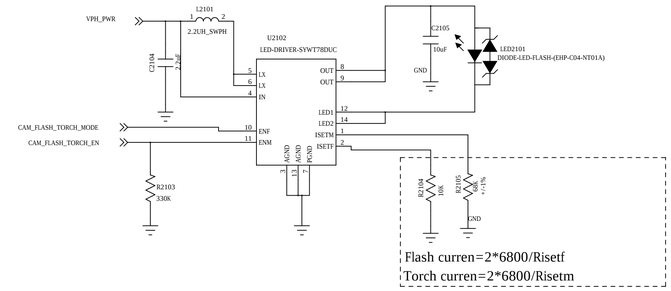
PIN		
1	GND	
2	MCLK	
3	GND	
4	MDN1	
5	MDP1	
6	GND	
7	MCN	
8	MCP	
9	GND	
10	MDNO	
11	MDPO	
12	GND	
13	GND	
14	GND	
15	AVDD	2.8V
16	GND	
17	DOVDD	1.8V
18	DVDD	1.2V
19	GND	
20	SCL	
21	SDA	
22	GND	
23	PWDN	
24	RESET	

Sub Camera



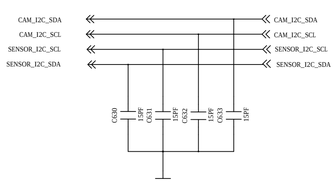
FRONT_camera

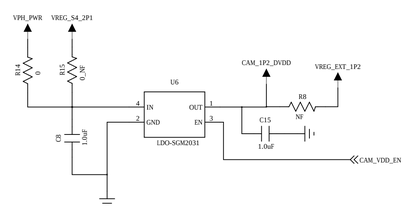
Main Camera / Sub Camera share power domain design
should double check the voltage level is compatible

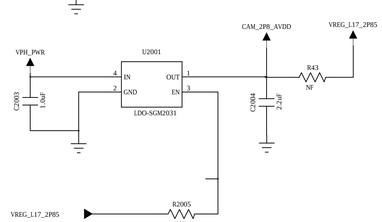


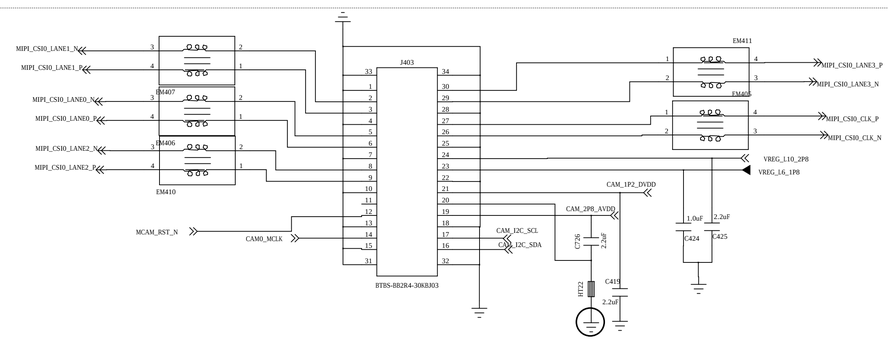
FLASH LED DRIVER

Main Camera / Sub Camera share power domain design
should double check the voltage level is compatible









Rear Camera: 8Mp
Module:
Sensor: OV8865

I2C Address	
Write	0x6C
Read	0x6D

Power on sequence: L6(DOVDD) must before L17(AVDD)

Main Camera

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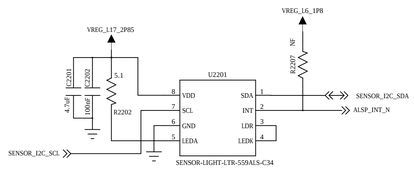
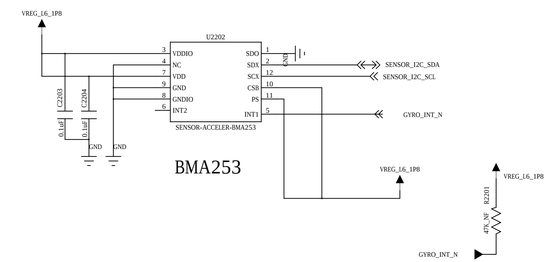


i2c slave add:0x23

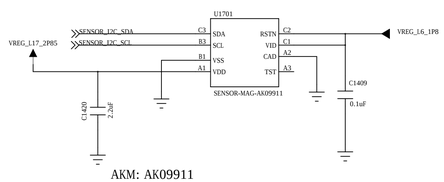
ALS+PS+IR

G-Sensor



BMA253

M-Sensor



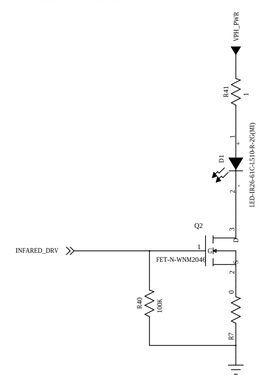
AKM: AK09911

I2C Address@CAD=0	
Write	0x18
Read	0x19

I2C Address@CAD=1	
Write	0x1A
Read	0x1B

Power on sequence: L6/L17 can be applied in any order

INFARED LEDS



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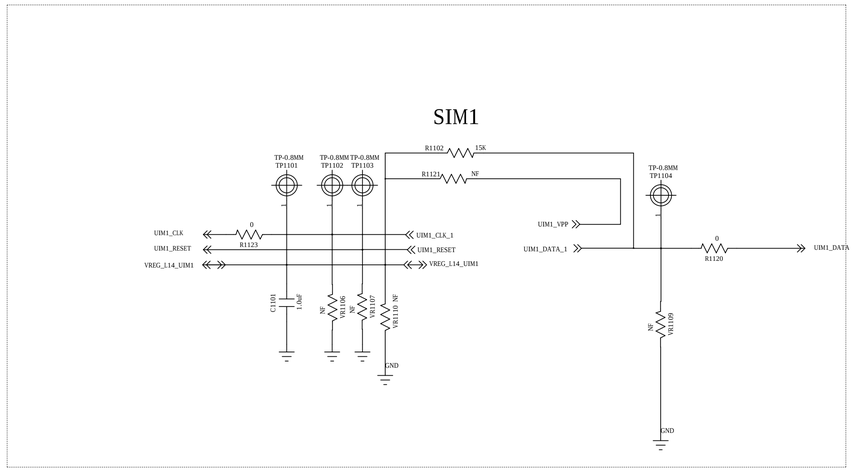
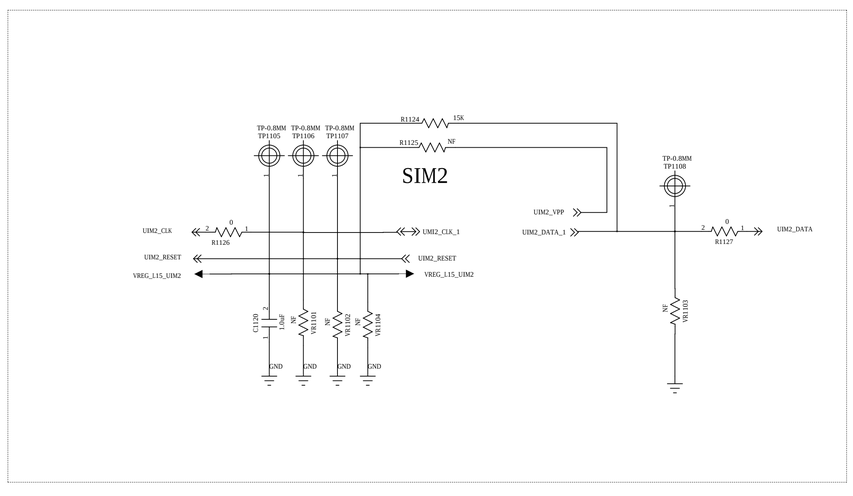
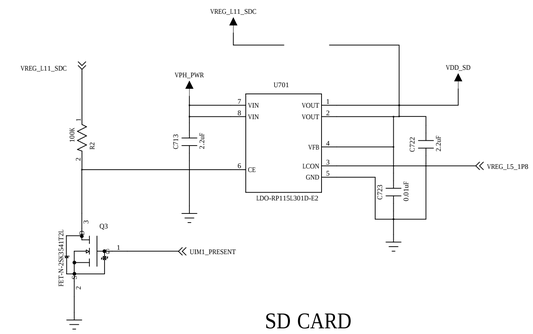
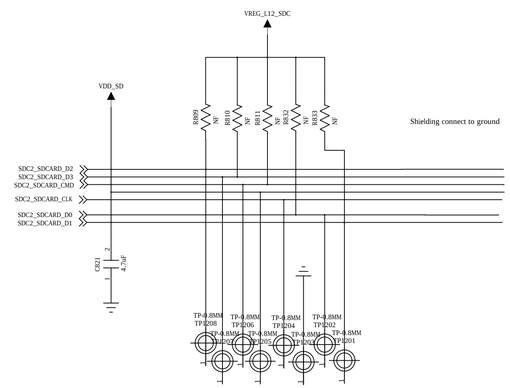


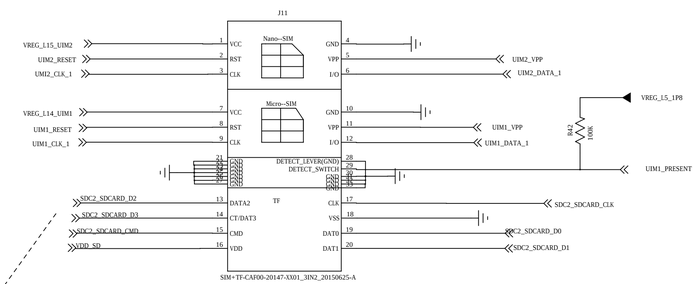


Vout=3.0V,I-lim=1A



SD CARD





This int should give to GPIO38/GPIO56/GPIO60

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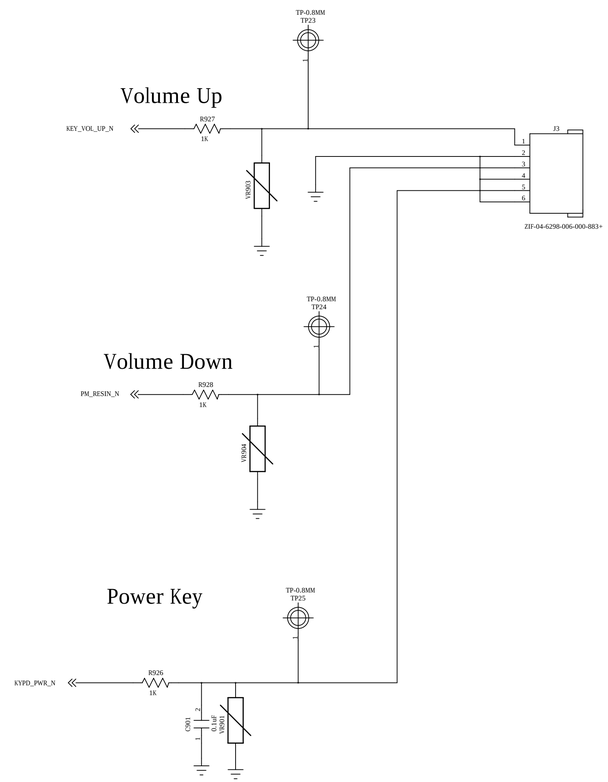

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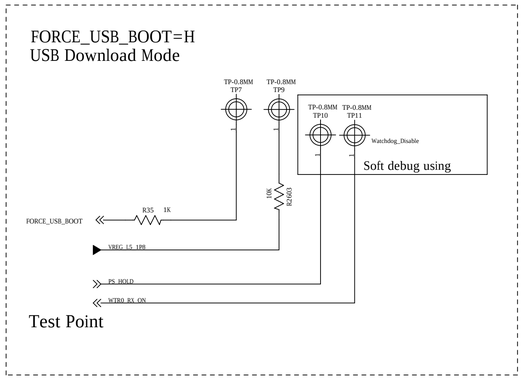
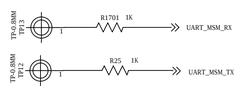
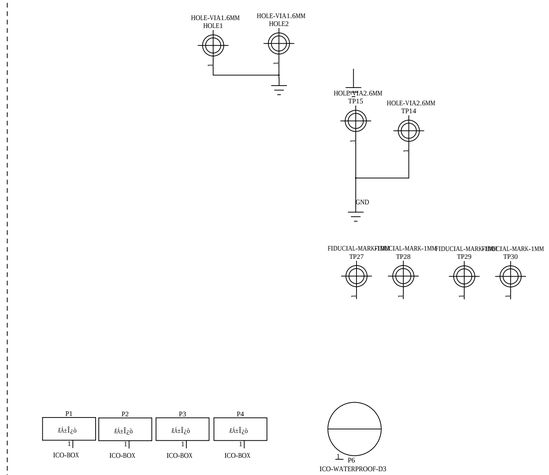




JTAG DEBUG



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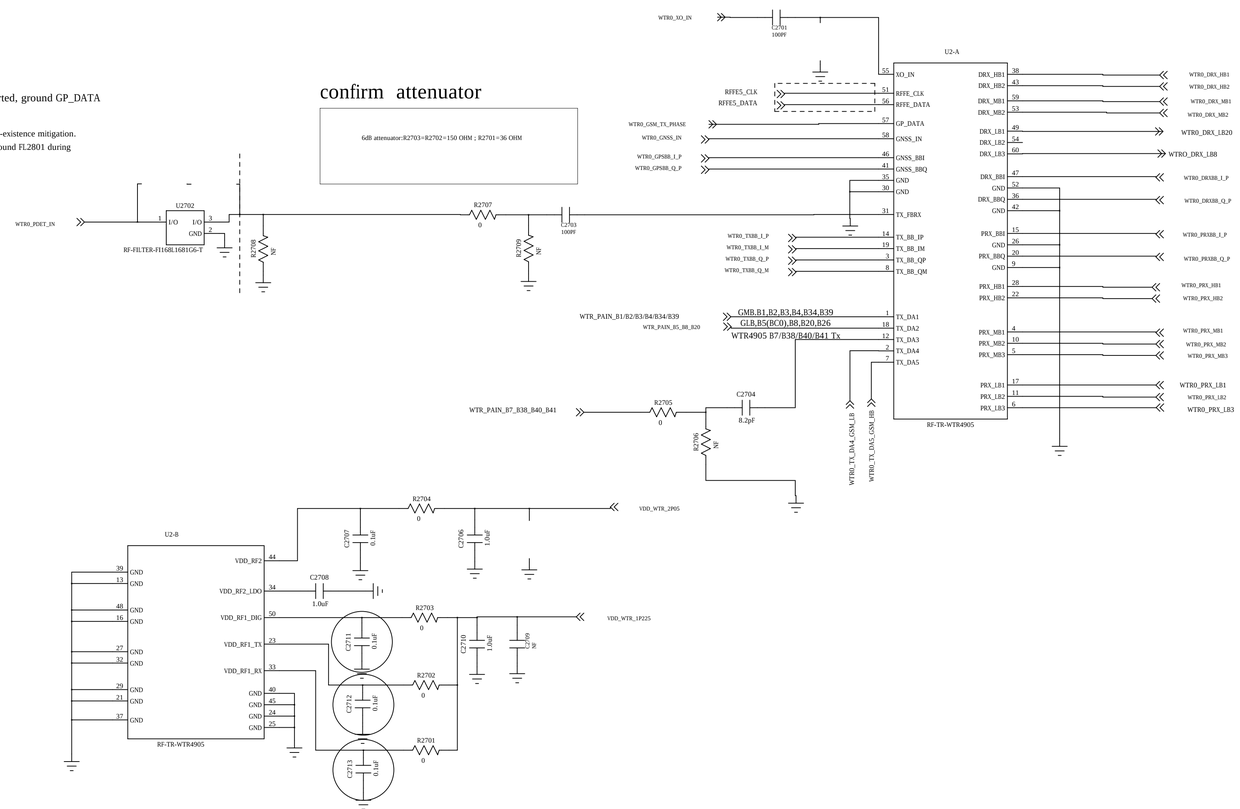
WTR4905 CONTROL, PWR & GND

If GSM is not supported, ground GP_DATA

Note: FL2801 is a 5GHz LPF for Wi-Fi co-existence mitigation.
Recommend a bypass option around FL2801 during
evaluation until proven.

confirm attenuator

6dB attenuator:R2703=R2702=150 OHM ; R2701=36 OHM



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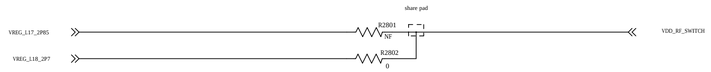

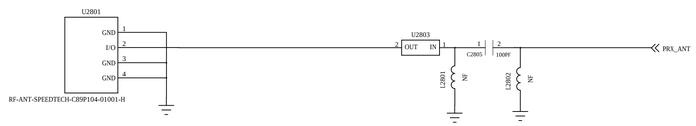

	ANT_SWITCH_CTL0	ANT_SWITCH_CTL1
TRX_B7		
TRX_B40		
QFE2320_ANT		
TRX_B38_41		

	ANT_SWITCH_CTL0	ANT_SWITCH_CTL1
TRX_B7		
TRX_B40		
QFE2320_ANT		
TRX_B38_41		

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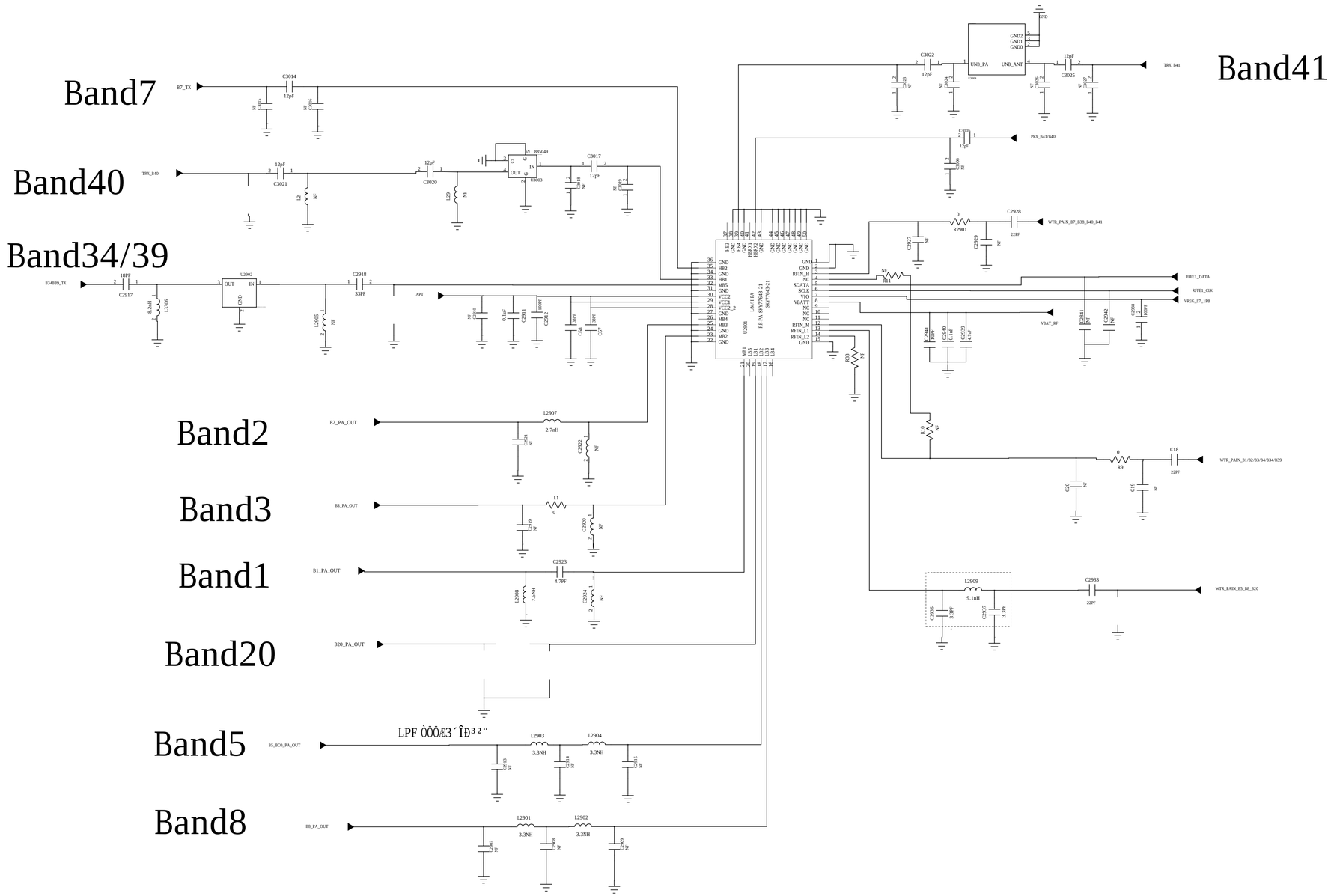

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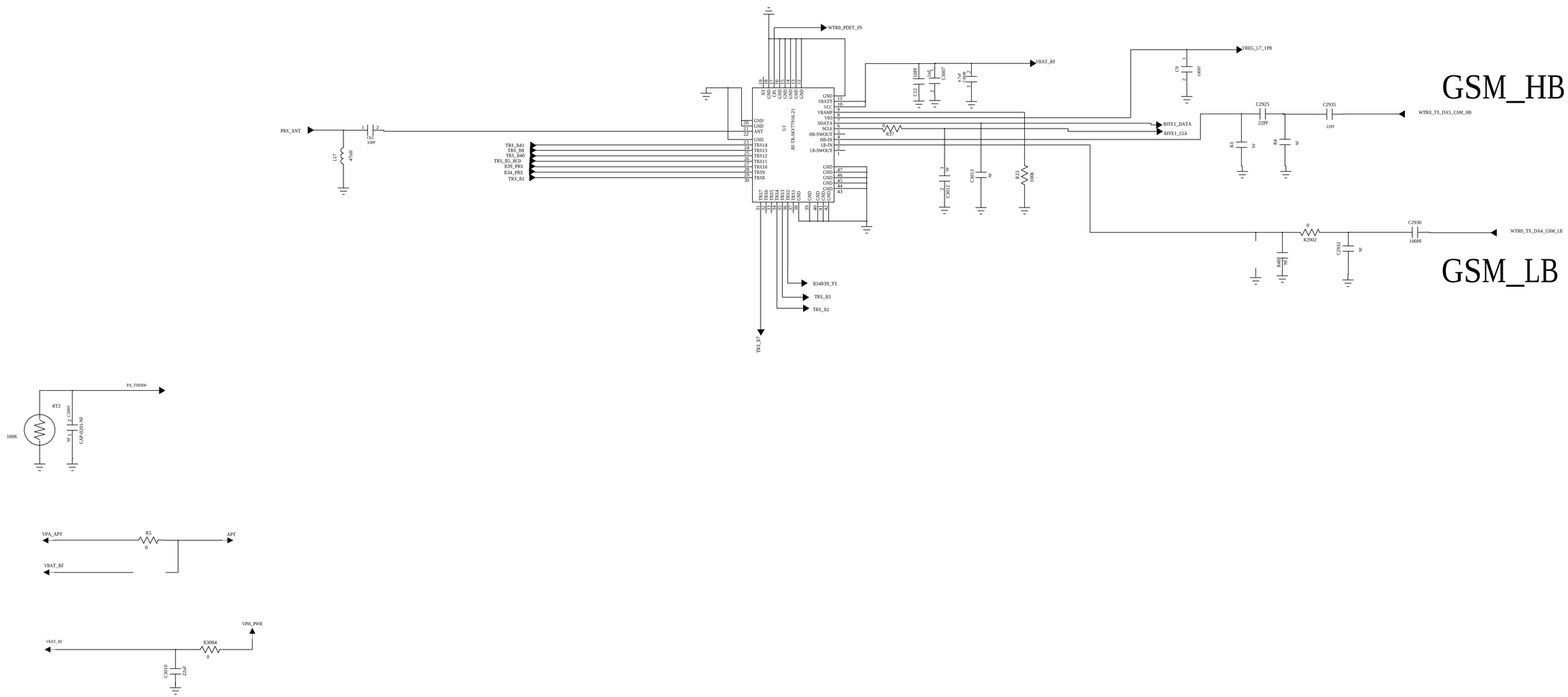

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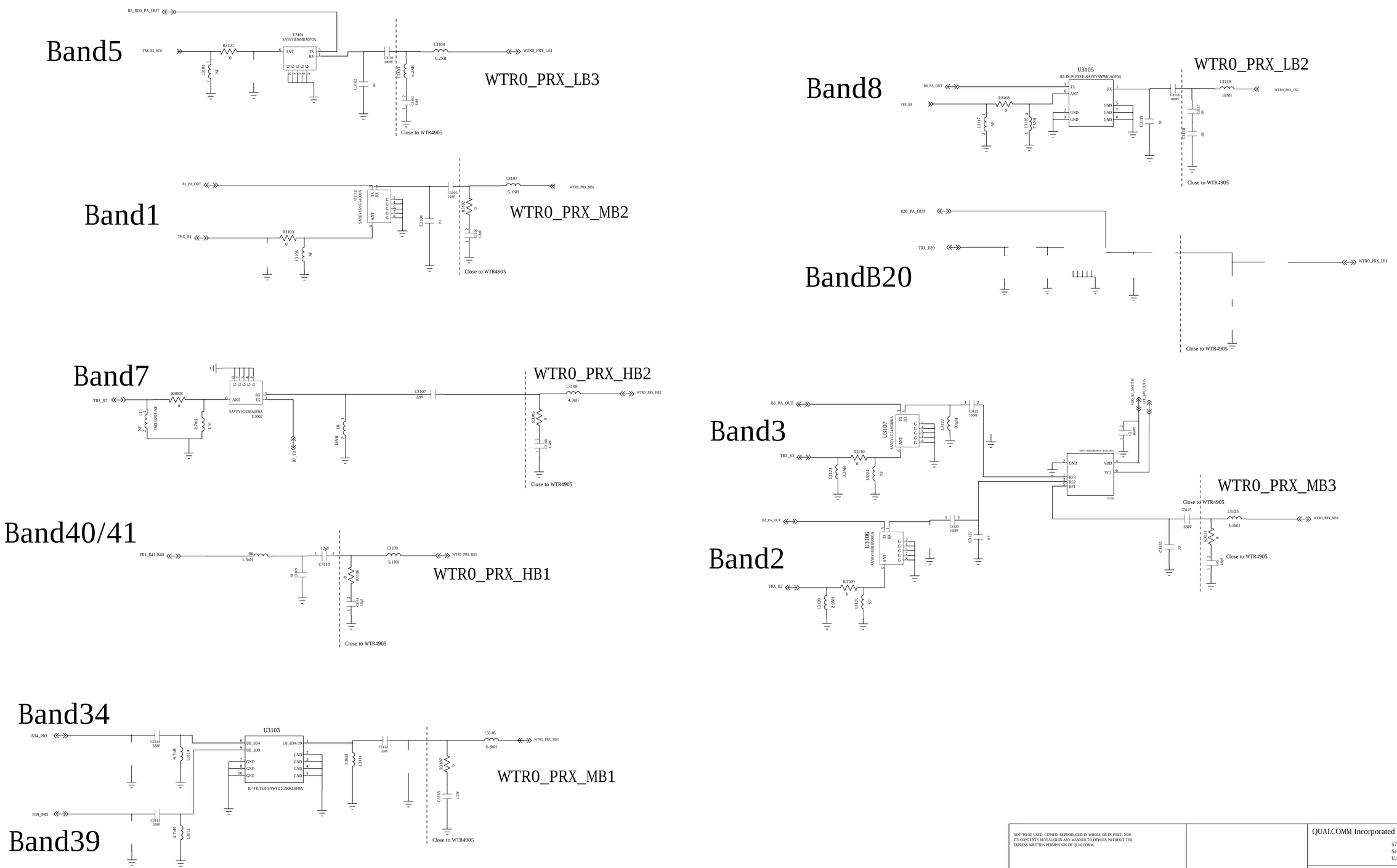

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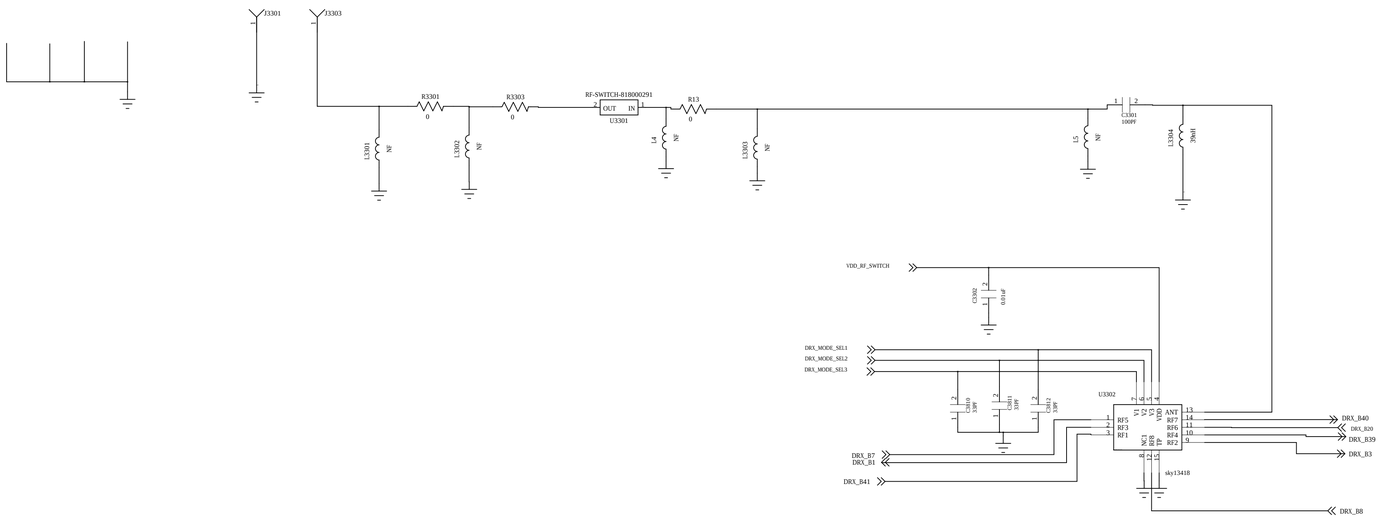

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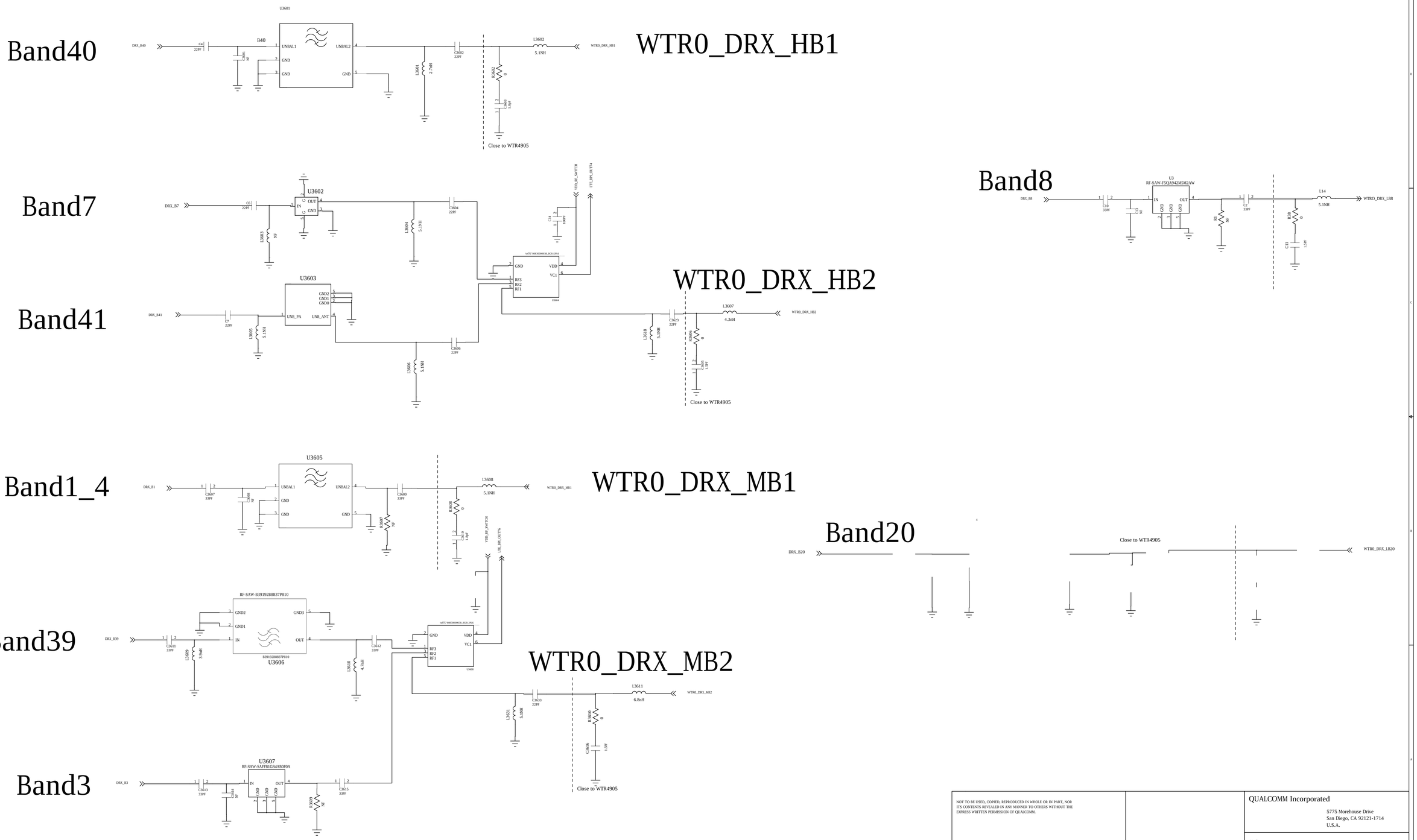

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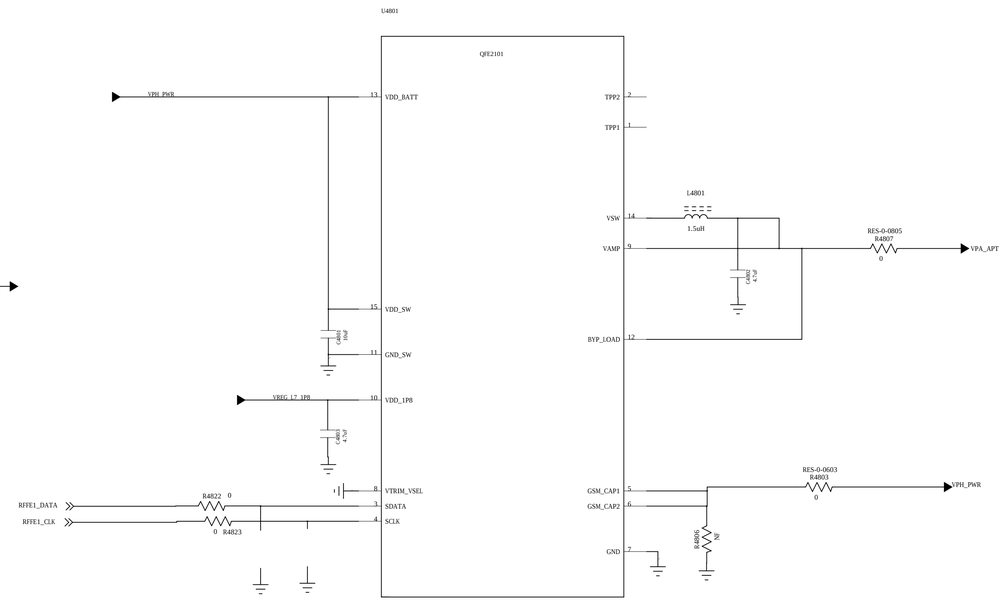
Note: Use a signle low impedance power plane/fill VPA for all ET PA VCC1/VCC2.

Refer to 80-NA681-91 rev.B or later revisions for more layout details.



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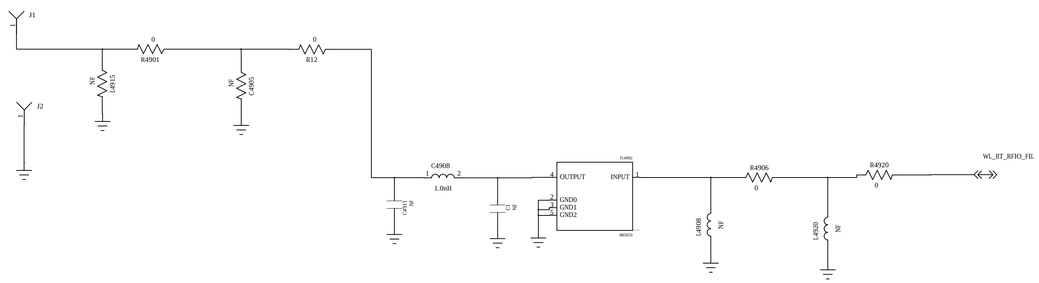
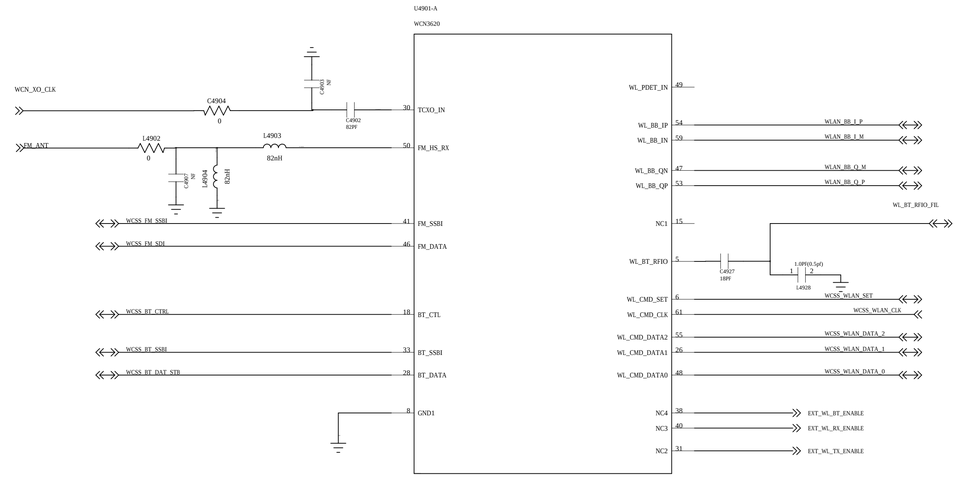
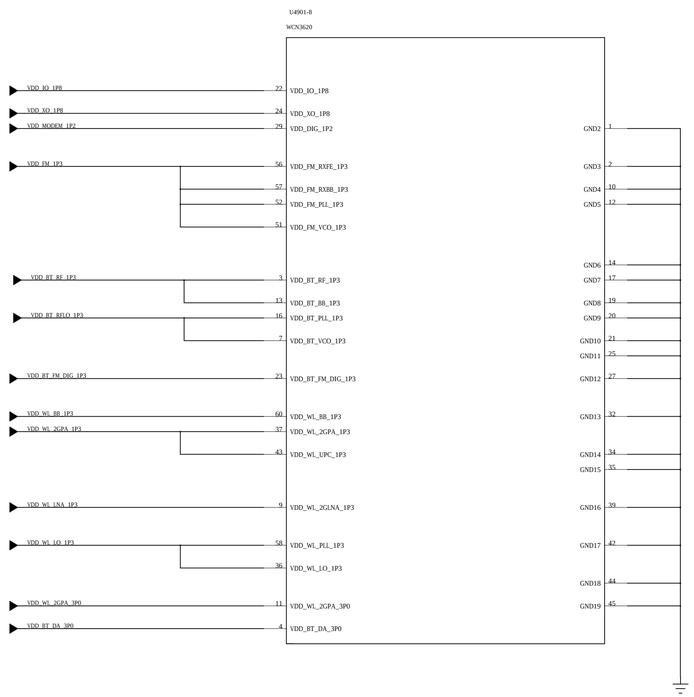
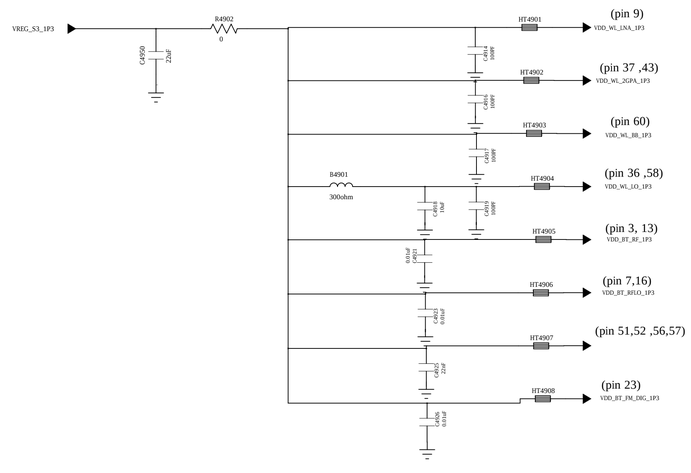
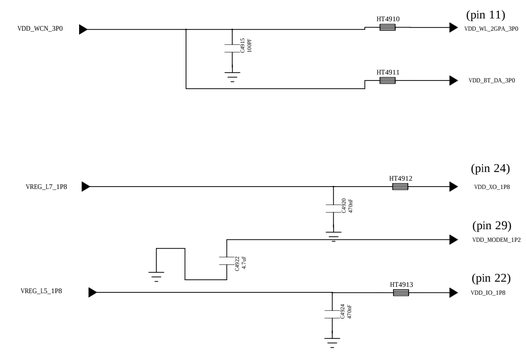
WIFI/BT











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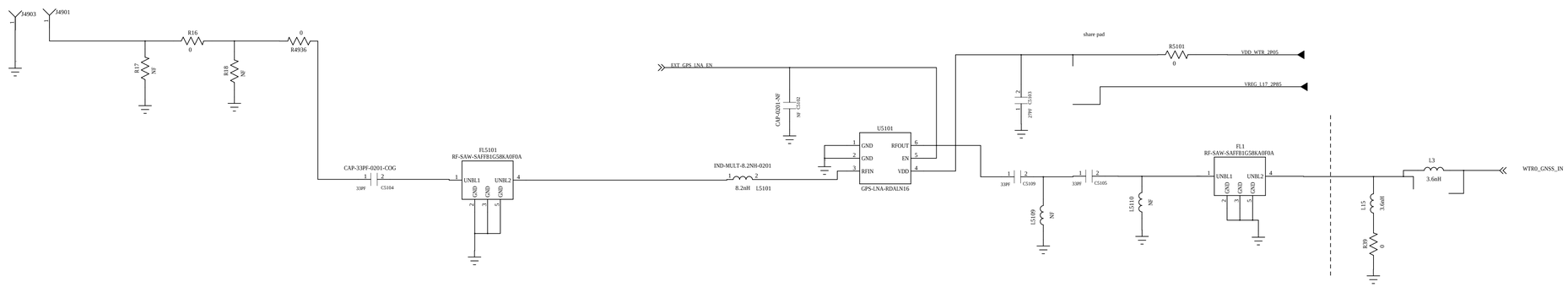

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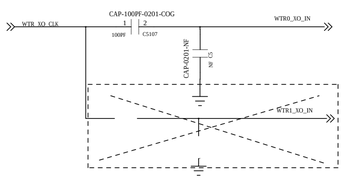

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